

## ABSTRACT OF THE DISCLOSURE

The invention includes a method of forming an array of memory cells. A series of capacitor constructions is formed, with the individual capacitor constructions having storage nodes. The capacitor constructions are defined to include a first set of capacitor constructions and a second set of capacitor constructions. A series of electrically conductive transistor gates are formed over the capacitor constructions and in electrical connection with the capacitor constructions. The transistor gates are defined to include a first set that is in electrical connection with the storage nodes of the first set of capacitor constructions, and a second set that is in electrical connection with the storage nodes of the second set of capacitor constructions. A first conductive line is formed over the transistor gates and in electrical connection with the first set of transistor gates, and a second conductive line is formed over the first conductive line and in electrical connection with the second set of transistor gates. The invention also includes an array of memory cells.